VLSI DESIGN SKILLING PROJECT ABSTRACT

**Title:** RF Design of 2.4GHz Bluetooth LNA using 45nm CMOS Technology

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* **Tool:** Cadence Virtuoso
* **Technology:** CMOS

**Abstract:**

The aim of this is to build a high Bluetooth low-noise amplifier that operates properly in the frequency range between 2.4 GHz & 2.5 GHz, using the 45nm CMOS technology. In this a comparison is made between two common topologies, the common-source (CS) amplifier & the cascode CS amplifier. Both circuits are designed to achieve the highest within the allowable power budget & also maintain suitable impedance matching. Both circuits are tested through software simulations using Cadence Virtuoso’s Analog Design Environment (ADE).

**Introduction:**

In any radio-frequency (RF) integrated circuit system, the low-noise amplifier (LNA) is usually the first active stage of the receiver, thus making its design of crucial importance. The receiver receives a weak signal at the antenna that, in order to be utilized, must be amplified before being processed on in the following stages, making the small-signal AC gain (AV) a critical design specification of the LNA. The received signal also contains noise that is added to it before reaching the receiver. Completely removing the noise is impossible, but with careful design, the amount of noise added & the amount by which the noise is amplified with respect to the desired signal can be decreased by minimizing the amplifier’s noise figure (NF). The input reflection coefficient. This parameter shows the amount of signal power transferred from the input to the output. To keep S11 at a minimum value (for maximum power transfer), careful matching between the antenna & the LNA is ensured using a matching circuit. Additionally, the linearity of the LNA’s circuit determines the maximum allowable power level of the input.